Impact of single pMOSFET dielectric degradation on NAND circuit performance

D. Estrada a, M.L. Ogas a, R.G. Southwick III a, P.M. Price b, R.J. Baker a, W.B. Knowlton a,b,*

a Electrical and Computer Engineering Department, Boise State University, 1910 University Dr., Boise, ID 83725, USA
b Materials Science and Engineering Department, Boise State University, 1910 University Dr., Boise, ID 83725, USA

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Abstract

Degradation of CMOS NAND logic circuits resulting from dielectric degradation of a single pMOSFET using constant voltage stress has been examined by means of a switch matrix technique. As a result, the NAND gate rise time increases by greater than 65%, which may lead to timing errors in high frequency digital circuits. In addition, the NAND gate DC switching point voltage shifts by nearly 11% which may be of consequence for analog or mixed signal applications. Experimental results for the degraded pMOSFET reveal a decrease in drive current by approximately 43%. There is also an increase in threshold voltage by 23%, a decrease in source-to-drain conductance of 30%, and an increase in channel resistance of about 44%. A linear relationship between the degradation of the pMOSFET channel resistance and the increase in NAND gate rise time is demonstrated, thereby providing experimental evidence of the impact of a single degraded pMOSFET on NAND circuit performance.

1. Introduction

The effects of dielectric breakdown mechanisms on inverter circuit performance have received recent attention [1–8], yet experimental results (i.e., not simulated) on these effects on other logic gates, such as the NAND gate, are negligible. Furthermore, the focus of reliability studies on the inverter logic circuit has involved the detrimental aspects of a circuit level stress on the DC voltage transfer characteristics (VTC) exclusive of circuit response in the time-domain [1,2,7,8]. In these studies, the type of degradation induced in one or both of the MOSFETs can only be inferred as electrical access to each individual MOSFET was not possible. However, it has been shown that directly characterizing each individual MOSFET before and after stress is possible by employing a switch matrix technique when configuring simple integrated circuit building blocks (SICBBS) [3,6]. This method has been used to investigate inverter logic circuit performance following degradation of a single MOSFET (or both MOSFETs) [4] in which degradation of MOSFET parameters was examined and directly correlated to inverter degradation in the voltage–time-domain ($V$–$t$). The switch matrix technique has also been employed in a preliminary investigation on the degradation of rise time ($t_r$) in the NAND gate [9]. This study expands the preliminary investigation of NAND gate performance following pMOSFET degradation by comparing NAND circuit degradation in the DC and $V$–$t$ domains. Additionally, the correlation between pMOSFET degradation and NAND circuit reliability is experimentally and mathematically investigated. Moreover, the capacitive load associated with the switch matrix technique is addressed using experimental, mathematical, and simulation approaches.

Ogas et al. have proposed circuit performance can deteriorate before traditional gate oxide breakdown (GOB) events occur such as soft breakdown (SBD) or hard breakdown (HBD) [4]. Similarly, NAND gate and full adder...
circuit simulations performed by Carter et al. suggest that logic circuits are affected dynamically by gate oxide degradation [10]. Their analyses present data that result in timing delays of NAND circuits and propagation of these timing delays through the logic path of a full adder circuit following a progressive GOB [10]. In addition, Hawkins et al. suggest IC parameter variance becomes a greater concern for the timing of logic circuits with the scaling of technology nodes through their simulations of NAND logic circuits [11]. However, to the authors’ knowledge, experimental studies to support these simulations have yet to be performed on devices with ultra-thin oxides.

It is well known that device speed increases as MOSFET gate dielectric thickness ($t_{OX}$) is scaled down. However, with scaling, detrimental effects resulting in earlier dielectric breakdown, such as increased gate leakage current and increased defect generation become a greater concern. Consequently, it has become increasingly important to identify which components are most susceptible to dielectric degradation as circuit engineers continue to design with devices utilizing thinner gate oxides. Our study investigates the NAND logic circuit performance following degradation of devices with $t_{OX}$ of 2.0 nm. Of particular interest is the reliability assessment of low-level oxide degradation (e.g., negative bias temperature instability [12,13], time dependent dielectric breakdown [14], stress induced leakage current [15], progressive breakdown [16,17], etc.), termed wear out in this paper [18], which may provide insight as to the critical degradation limit for digital circuit failure. This paper examines the effect of wear out in one pMOSFET on NAND gate performance. The focus of this study is not on the identity of the specific physical degradation mechanism (e.g., NBTI [12,13], TDDB [14], SILC [15] or progressive breakdown [16,17], etc.), which is left to the discretion of the reader, but on the impact of the induced device degradation on the NAND circuit response. To this end, a possible connection between MOSFET degradation and circuit performance may be established through the widely used relationship between circuit $t_r$ and MOSFET channel resistance, $R_{ch}$, in the design of logic circuits, given by:

$$t_r \propto R_{ch}C_L$$

where $C_L$ is the load capacitance on the logic circuit [19,20]. Based on our investigation of Eq. (1), we provide experimental evidence that directly correlates gate oxide wear out effects on the channel resistance of one pMOSFET to the NAND logic circuit rise time.

2. Experimental

2.1. Devices and measurements

The metal oxide semiconductor (MOS) devices used in this study are fabricated using 0.1 μm CMOS technology with a $t_{OX}$ of 2.0 nm. The pMOSFET and nMOSFET devices configured in the NAND circuit have an oxide area ($A_{OX}$) of $1 \times 10^{-8}$ cm$^2$ with a width and length of 10 μm and 0.1 μm, respectively. The dielectric type is SiO$_2$. Measurements are obtained using a semiconductor characterization system described in previous studies [6]. Dielectric degradation is induced in a single pMOSFET by applying a constant voltage stress (CVS) of −4 V to the gate of the device (Fig. 1) [21]. Further description of the measurement and choice of applied voltage is reported in previous work [4]. CVS occurs in cycles of 600 s for five consecutive cycles, with interruptions for device and circuit characterization. The remaining three MOSFETs are not stressed. All measurements are conducted at 298 K.

Data have been collected and analyzed for 6 NAND gates with a single degraded pMOSFET configured in 1 of 2 positions through the switch matrix technique, as illustrated in Fig. 2. Table 1 summarizes all four NAND logic configurations, which are labeled with the pMOSFET position followed by the I/O state. Configurations 1–3 and 2–1, shaded in Table 1, correspond to transitions in the NAND logic. The results are presented for these two configurations in which device degradation affects the circuit performance in the voltage–time-domain ($V$–$t$). Specific to the NAND circuit, $V$–$t$ data and voltage transfer characteristics (VTCs) are measured following each stress cycle. The $V$–$t$ results allow for the evaluation of rise time ($t_r$) by taking the difference in time from 90% to 10% of the output voltage [20].

Data collected for the degraded pMOSFET includes maximum drain current ($I_{D,max}$), threshold voltage ($V_{TH}$), maximum transconductance ($G_{M,max}$), off-current ($I_{off}$), and small-signal source-to-drain conductance ($g_{sd,m}$). The
of heavily loading mixed signal circuits include charge pumps and loop filters (e.g., digital phase-locked loops or DPLL). The capacitive load, $C_L$, for these circuits can be 1 pF or larger. It would be of definite interest to determine if the change in $t_r$ of a NAND circuit, measured under the heavy $C_L$ of the switch matrix technique, can be directly attributed to the oxide degradation of one MOSFET in the NAND gate. Theoretically, this might be possible by examining the well known relationship of $t_r$ shown previously in Eq. (1). If a NAND gate is under a large load capacitance, which remains constant, then a change in $R_{ch}$ can be directly related to a change in $t_r$. Hence, Eq. (1) can then be written in terms of a change in $R_{ch}$ ($\Delta R_{ch}$) given by:

$$\Delta t_r \propto \Delta R_{ch} C_L$$

or,

$$\Delta t_r \propto (R_{ch,fresh} - R_{ch,wearout}) C_L.$$ 

(3)

Consider the following case in which $C_L$ can be increased or decreased prior to or after circuit operation but remains constant during circuit operation or measurement (i.e., a different output circuit on the NAND). A question arises as to whether or not the change in $C_L$ produces a change in $\%\Delta t_r$ (where % signifies fractional percent). Insight to this question is gained by writing Eq. (1) in terms of $\%\Delta t_r$:

$$\%\Delta t_r \propto \frac{\Delta t_r}{t_{r,fresh}} \propto \frac{\Delta t_r}{R_{ch,fresh} C_L}.$$ 

(4)

Substituting Eq. (3) into (4) provides:

$$\%\Delta t_r \propto \frac{(R_{ch,fresh} - R_{ch,wearout}) C_L}{R_{ch,fresh} C_L}. \propto \frac{R_{ch,wearout}}{R_{ch,fresh}} \propto \%\Delta R_{ch}.$$ 

(5)

Eq. (5) reveals that $\%\Delta t_r$ is independent of $C_L$. The result of Eq. (5) is rather simplistic and may leave the reader with doubt to its outcome. Hence, SPICE simulations were performed that demonstrate, for changes in $C_L$ ranging from 10 fF up to 1 nF (but holding $C_L$ constant during each simulation), $\%\Delta t_r$ remains the same, Fig. 3.

Degradation was simulated in a single pMOSFET by increasing the threshold voltage parameter, $V_{THO}$, of a 50 nm CMOS process BSIM 4 SPICE model to match the $\%\Delta V_{TH}$ increase observed in the experimental data following oxide wear out in a single pMOSFET. $V_{THO}$ was chosen because of its relationship to $R_{ch}$ as shown later. The NAND circuit investigated in this study was simulated using LT SPICE. Voltage-time-domain simulations were performed for the NAND circuits using the capacitive load of the Switch Matrix Technique (i.e., approximately 900 pF). Fig. 4 illustrates the typical correlation between simulated and experimental results. The switch matrix technique is well suited to examine the reliability of simple integrated circuit building blocks (SICBB) since the $C_L$ for this technique is about 900 pF (within the range of simulations) and remains constant throughout testing. We have also
performed experiments in which the $C_L$ on the NAND gate was reduced by nearly an order of magnitude and obtained the same results (within a standard deviation) as with the switch matrix technique.

Using the switch matrix technique, we examine the effect of oxide wear out in a pMOSFET on the functionality of a NAND logic circuit. It is shown for NAND gates, which can be heavily loaded by circuits such as output buffers, charge pumps and loop filters, that pMOSFET oxide wear out is significantly disruptive to NAND gate performance.

3. Results

The NAND circuit and pMOSFET results reported include the $\%\Delta$ from fresh to wear out in terms of the mean value. The pMOSFET results are summarized in Table 2. For both the NAND circuit and the pMOSFET only the $\%\Delta$ mean is referenced in the following subsections.

3.1. NAND circuit

Following degradation of a single pMOSFET, both $V_t$ and VTCs are examined for configurations 1–3 and 2–1 (Table 1). These configurations are the only two configurations exhibiting effects from pMOSFET degradation as expected. Fig. 5 shows the NAND $V_t$ response for circuit configurations (a) 1–3 and (b) 2–1. The NAND $V_t$ response for Fig. 5a and b shows an increase in $\%\Delta_t$ of approximately 68%, relative to the fresh response. Fig. 6 shows the NAND VTCs for configurations (a) 1–3 and (b) 2–1, in which a shift to the left, starting from the fresh condition, is observed in the voltage switching point ($%\Delta V_{SP}$) by approximately 11% and 9%, respectively. Fig. 7 shows box plots with respect to stress cycle of (a) $%\Delta_I$ and (b) $%\Delta V_{SP}$. The mean values of each box plot are connected by a solid line, indicating a gradual increase in mean values for each tested circuit with increased degradation as illustrated in Figs. 5 and 6. A gradual increase in the value of the interquartile range with increased oxide wear out is also observed.

3.2. pMOSFET

After 3000 s of CVS, the pMOSFET DC characteristics show a decrease in $\%\Delta I_{D,\text{max}}$ (Fig. 8) by 43%. Fig. 9 reveals an increase in $%\Delta V_{TH}$ by 23%, and a decrease in $%\Delta G_{M,\text{max}}$ (inset of Fig. 9) by 26%. Additionally, a decrease in $%\Delta I_{off}$ by 82% is observed (Fig. 10). The $%\Delta g_{sdm}$ in Fig. 11 is shown to decrease by 30% (measured at $V_{SG} = V_{DD} = 1\text{V}$). In Fig. 12, an increase is observed in $%\Delta R_{dh}$ of approximately 44%.

<table>
<thead>
<tr>
<th>Table 2</th>
<th>pMOSFET device statistics</th>
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<tbody>
<tr>
<td>$I-V$ parameter</td>
<td>Mean (%)</td>
</tr>
<tr>
<td>$%\Delta I_{D,\text{max}}$</td>
<td>43</td>
</tr>
<tr>
<td>$%\Delta V_{TH}$</td>
<td>23</td>
</tr>
<tr>
<td>$%\Delta G_{M,\text{max}}$</td>
<td>26</td>
</tr>
<tr>
<td>$%\Delta I_{off}$</td>
<td>82</td>
</tr>
<tr>
<td>$%\Delta g_{sdm}$</td>
<td>30</td>
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4. Discussion

4.1. NAND circuit

The method that was chosen for testing the NAND gate induces a pulsed waveform on one input while applying a constant voltage to the other input. Thus, simplifying the experiment by isolating the switching transistors in the NAND gate to one pMOSFET and one nMOSFET (cases A and B described by Taur and Ning) [24]. This method prevents both pMOSFETs from switching simultaneously and allows for easier analysis of the impact of the degraded pMOSFET on the NAND circuit response. It is shown following stress of a single pMOSFET, the degree of degradation observed in the NAND time-domain response is more significant than the degradation exhibited in the VTCs under equivalent test conditions (Figs. 5 and 6).

Examining the data in Fig. 5 demonstrates that only $t_r$ of the NAND gate is affected, while the fall time ($t_f$) remains unchanged (Fig. 5). As reported by Stutzke et al., a degraded pMOSFET affects only the $t_r$ [3], hence a change in $t_f$ is not expected, nor is it observed. This can be explained by realizing that the pMOSFET is the “pull-up” device and the nMOSFET is the “pull-down” device, as described by Taur and Ning [24]. Furthermore, comparison of the $\% \Delta t_r$ results for configuration 1–3 (Fig. 5a) to the $\% \Delta t_f$ results for configuration 2–1 (Fig. 5b) reveals that a single degraded pMOSFET has an equivalent effect on NAND circuit performance in the $V–t$ domain regardless of circuit configuration. This can be explained by realizing that by holding one input of the
NAND gate at VDD while the other input is pulsed, the pull-up operation of a two input NAND gate is similar to that of a CMOS inverter [24]. Hence, for both configurations 1–3 and 2–1, the impact of single pMOSFET oxide wear out on the NAND logic gate performance in the V–t domain is comparable to findings reported in similar work involving the Inverter logic circuit [4]. Moreover, the data in Fig. 5 may be examined statistically over the stress cycles as shown in Fig. 7a. Statistical examination of the data reveals valuable information concerning trends in the circuit V–t response (Fig. 7a). The data in Fig. 7a indicate the %Δτ increases steadily and substantially for each circuit. For all circuits tested, the same trend in %Δτ is observed, which is a sublinear increase in %Δτ with increasing stress cycle.

A similar correlation can be made for the NAND VTCs from Fig. 6, in which a leftward shift of the VSP is directly related to a decrease in I_D,max of approximately 43% with increasing wear out. I_D,max data is measured at V_D = VDD (encircled). The gate voltage is held constant at −1 V throughout the test.

Fig. 7. Box plots of (a) voltage-time-domain (V–t) and (b) voltage transfer characteristics (VTCs) for configuration 1–3 versus stress cycle. The numbers illustrate the different circuits tested (i.e., all four MOSFETs used to construct the NAND circuit are different and unstressed before testing). Each individual box plot has a range from the minimum measured value to the maximum measured value. The box represents the interquartile range. The mean values of each individual box plot are depicted by a solid square and are connected by a solid line. The median is illustrated by a horizontal solid line in the box. Configuration 2–1, not shown, yields comparable results. The %Δτ, from fresh to stress cycle E for this configuration is approximately 68% while the %ΔVSP from fresh to stress cycle E is only 11% (by mean). A gradual increase in the value of the interquartile range with increased stress time is observed for both (a) %Δτ and (b) %ΔVSP.

Fig. 8. Typical pMOSFET drain current versus drain voltage (I_D – V_D) results for fresh through stress cycle E showing a decrease in I_D,max of approximately 43% with increasing wear out. I_D,max data is measured at V_D = VDD (encircled). The gate voltage is held constant at −1 V throughout the test.

Fig. 9. Typical pMOSFET linear drain current versus gate voltage (linear I_D/C0 V) results for fresh through stress cycle E, in which an increase in threshold voltage (V_TH) of approximately 23% is observed from fresh to stress cycle E. The inset illustrates that the corresponding maximum transconductance (G_M,max) decreases by approximately 26% and shifts to more negative voltages with increased wear out (only fresh and stress cycle E are presented). Throughout the test, drain voltage is held constant at −50 mV. V_TH is measured using the linear extrapolation method [22].
pMOSFET and undamaged nMOSFET shifted the $V_{SP}$ to the left while a degraded nMOSFET and undamaged pMOSFET shifted the $V_{SP}$ to the right [4,6]. Additionally, comparison of the $\%\Delta V_{SP}$ data for configurations 1–3 and 2–1 (Fig. 6a and b) demonstrates a single degraded pMOSFET has a similar effect on NAND circuit performance in the DC domain regardless of circuit configuration. This can also be explained by realizing that by holding one input of the NAND gate at VDD while the other input is pulsed the pull-down operation of a two input NAND gate is similar to that of a CMOS inverter [24]. However, it is important to note that configuration 2–1 is most comparable to the CMOS Inverter as VTC results for configuration 1–3 could be influenced by the body effect associated with stacked nMOSFET devices [24]. Hence, the observed $\%\Delta V_{SP}$ for configuration 2–1 is most comparable to the $\%\Delta V_{SP}$ reported in similar work involving the Inverter logic circuit [4]. Statistical examination of the data in Fig. 6a provides the box plots in Fig. 7b where the $\%\Delta V_{SP}$ data for each circuit are shown over the stress cycles. The $\%\Delta V_{SP}$ depicts a sublinear increase as well, thus further suggesting the validity of the trends in both $\%\Delta t_r$ and $\%\Delta V_{SP}$ with stress time.

The evolution of $\%\Delta t_r$ and $\%\Delta V_{SP}$ may be described by the slope of the curves which connect the box plot mean values as shown in Fig. 7a and b. Initially, the slopes of these curves are large but decrease to a relatively constant value. This tendency correlates to the pMOSFET gate leakage current progression with respect to degradation encircled in the “Region Investigated” in Fig. 13. The first cycle of wear out shows the greatest increase in gate leakage current while subsequent wear out exhibits less leakage current changes. It is interesting to note that the $\%\Delta t_r$ increase is a factor of four or more greater than that observed for the $\%\Delta V_{SP}$ indicating that the circuit operation in the time domain is more affected by gate oxide wear out than for DC operation. Since a significant portion of circuit operation is in the time-domain, the greater sensitivity of $\%\Delta t_r$ to gate oxide wear out suggests that gate oxide wear out is more detrimental to digital circuit operation than to analog operation.
Similar observations were reported by Cheek et al. following inverter circuit analysis [6]. In addition, the degradation of the NAND \( V-t \) response with increased wear out reported in Section 3.1 are supported by the simulation work of Carter et al. in which GOB is simulated and the result is an increase in time delay for the NAND gate time-domain response [10].

4.2. pMOSFET

The evidence presented in Section 4.1 indicates that pMOSFET wear out causes a significant change in NAND gate circuit response. Consequently, the pMOSFET characteristics are examined to establish the cause of the large change in \( t_r \). The \( I_G-V_G \) data in Fig. 13 are substantiated by the Region Investigated highlighted in Fig. 1 where wear out is evident. A potential link between circuit performance and MOSFET degradation is that of \( t_r \) and \( R_{ch} \) (Eqs. (1) and (5)). To this end, \( R_{ch} \) is experimentally investigated. To obtain the values for \( \%\Delta R_{ch} \), an approach similar to that provided by Kong et al. [23] was applied in which an equation for \( g_{sdm} \) is derived. Kong’s derivation for \( g_{sdm} \), calculated from the DC drain current equation of an nMOSFET, is based upon the gradual channel approximation [23]. The gradual channel approximation remains valid for this study as only a small AC signal with a 0 V DC bias is applied to the drain when \( g_{sdm} \) is measured. Therefore, a similar derivation for the case of a pMOSFET results in

\[
g_{sdm} = \frac{1}{R_{SD} + \frac{1}{\beta(V_{SG} + V_{TH})}},
\]

where,

\[
R_{ch} = \frac{1}{\beta(V_{SG} + V_{TH})}
\]

and,

\[
\beta = \frac{\mu_{eff}C_{OX}W_{eff}}{L_{eff}}.
\]

\( R_{SD} \) is the total parasitic source and drain resistance measured in series with \( R_{ch} \). It can be assumed \( R_{SD} \) is small compared to \( R_{ch} \) [25,26] and remains fairly constant after CVS, as the majority of the pMOSFET degradation occurs in the channel [21]. Therefore, Eq. (4) can be reduced to

\[
g_{sdm} \approx \frac{1}{R_{ch}}
\]

or equivalently,

\[
R_{ch} \approx \frac{1}{g_{sdm}}.
\]

A correlation between \( \%\Delta R_{ch} \) and \( g_{sdm} \) can be derived from Eq. (10). \( \Delta R_{ch} \) can be written as

\[
\Delta R_{ch} \approx \frac{1}{g_{sdm, fresh}} - \frac{1}{g_{sdm, wearout}}.
\]

Using a common dominator, (11) can be written as

\[
\Delta R_{ch} \approx \frac{-\Delta g_{sdm}}{g_{sdm, fresh}g_{sdm, wearout}}.
\]

Dividing by \( R_{ch,fresh} \) to convert (12) to fractional percent change results in

\[
\%\Delta R_{ch} \approx \frac{\Delta R_{ch}}{R_{ch,fresh}} \approx \frac{-\Delta g_{sdm}}{g_{sdm, wearout}}.
\]

Using Eq. (13), \( \%\Delta R_{ch} \) was calculated using the small-signal conductance data. A statistical examination of the \%\Delta \( R_{ch} \) data (Fig. 12) reveals a sublinear increase similar to the \%\Delta \( t_r \) data (Fig. 7a). The evolution of \%\Delta \( R_{ch} \) may also be described by the slope of the line connecting the box plot mean values (Fig. 7a). Initially, the slope is large but decreases to a shallower value. However, it is most interesting to note that the \%\Delta \( R_{ch} \) trends for the devices (Fig. 12) are comparable with the \%\Delta \( t_r \) trends for the correlating circuits (Fig. 7a). To further discern the relationship between \%\Delta \( t_r \) and \%\Delta \( R_{ch} \) observed in Fig. 7a and Fig. 12, both the \%\Delta \( t_r \) data and \%\Delta \( R_{ch} \) data are plotted in Fig. 14. The linear fit of the data in Fig. 14 shows that \%\Delta \( t_r \) is directly proportional to \%\Delta \( R_{ch} \) through the relationship,

\[
\%\Delta t_r = 1.52 \times \%\Delta R_{ch}.
\]

The graphical relation observed in Fig. 14 demonstrates the validity of Eqs. (1) and (5) as well as the correlation between the trends illustrated in Fig. 7a and Fig. 12. Hence,
the change in channel resistance in the pMOSFET due to oxide degradation directly affects the rise time of the NAND logic gate.

Further insight into the degraded parameters affecting $R_{ch}$ is gained by following the derivation of Kong et al. relating $g_{sdm} = \frac{d}{dV_{sg}}$ as a linear function of gate voltage [23]. In the case of the pMOSFET, this relationship is expressed as

$$g_{sdm} = \sqrt{\beta_0} (V_{SG} + V_{TH})$$

where the zero gate-field gain factor, $\beta_0$, is proportional to $\beta$ through the well known relationship shown in Eq. (16) [27],

$$\mu_{eff} = \frac{\mu_0}{1 + \theta (V_{SG} + V_{TH})}$$

and $\theta$ is the gate-field mobility reduction factor. When the $g_{sdm}$ data are plotted according to Eq. (15) and a linear fit is applied to the various stress cycles (Fig. 15), it is observed that the slope of the linearization (i.e., $\sqrt{\beta_0}$) decreases with increased stress time. Furthermore, the shift in the $x$-axis intercept (i.e., $V_{TH}$) is approximately equal to the $V_{TH}$ shift measured using the linear extrapolation method (Fig. 9). Therefore, the results of the small-signal conductance measurement (Figs. 11 and 15) and the relationship expressed in Eq. (15) are substantiated by the data in Fig. 9, where a decrease in $G_{M,max}$ and shift in $V_{TH}$ are observed. Hence, the increase in $R_{ch}$ can be partly attributed to a decrease in $\mu_{eff}$, in accordance with Eq. (16). Since this study focuses on circuit response to MOSFET degradation, further investigation in the degradation mechanisms affecting $R_{ch}$ remains a topic that is beyond the scope of this paper.

5. Conclusions

Using a switch matrix technique, the results reported in this study show gate oxide wear out in one pMOSFET of a NAND logic circuit substantially degrades the circuit $V-t$ domain response and the VTCs. Additionally, it was found the NAND gate response in the $V-t$ domain is comparatively worse than the DC response. We have also proposed and shown the switch matrix technique can be employed in conjunction with a small-signal conductance measurement in characterizing the reliability of SICBBs, despite a relatively heavy capacitive load. A correlation between NAND logic circuit performance and degradation of pMOSFET parameters is established through analyses of $\%D_{\Delta t}$ and $\%D_{\Delta R_{ch}}$. Ultimately, the changes in $\Delta t$ may dramatically affect the ability of the NAND gate to execute logic properly, particularly in applications requiring high switching speeds.

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