Ch. 6 Devices – MOS Heterojunction – High K Dielectrics – Part 2

1. NVM High-k Devices (Charge Trap Memory) - NVM Floating Gate versus Charge Trap NVM
   What are three reasons why charge trap memory (e.g., SONOS) would be superior to floating gate memory? What are the names of the three dielectric layers in a charge trap layer? Which layer acts as a quasi-quantum well?

2. NVM High-k Devices (Charge Trap Memory) - Different Charge Trap Memory Stack Comparisons
   What is a better metric than the electron affinity for the charge trap layer (CTL)?
   If only comparing the EOT, V_t and C_{ox} of the three gate stacks, which stack is superior? Is the "Write" voltage a positive or negative gate voltage (V_g)?

- Extra credit: Why is the tunnel oxide on the charge trap memory (e.g., SONOS) so much thinner than the floating gate?