Electrical Characterization of
Solid State Ionic Memory Elements

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Abstract—Solid state ionic devices composed of metal doped glasses are among the promising new non-volatile memory technologies. The memory effect is based on polarity-dependent switching at small bias and current due to the electrodeposition of metal in the glassy electrolyte. Low voltage operation, high OFF/ON-ratios, and considerable scaling potential make this technology interesting for memory applications. In this paper, we present the results of extensive electrical characterizations from test-chips jointly processed and characterized at Arizona State University and at Infineon Technologies. The chips incorporate variations in feature size from the micrometer scale down to a hundred nanometers. The measurements address important topics for memory applications such as speed, retention, and endurance. We discuss the benefits as well as the challenges of this technology from its current stage of development.

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1. INTRODUCTION TO THE TECHNOLOGY

The semiconductor memory market has been characterized by constantly increasing demand for devices and bit densities for many years. The established technologies such as DRAM, SRAM, and Flash have specific shortcomings such as volatility (DRAM), size (SRAM) or limited endurance (Flash). Up to now there is no one technology which can fulfill all requirements of the different applications simultaneously. This stimulates work on novel memory technologies ultimately aimed at combining various desirable characteristics in one scalable device [1], [2].

Solid state ionic memory is among the promising new non-volatile memory technologies. It utilizes solid state electrochemistry at the nanoscale in certain materials, generally referred to as solid electrolytes [3]. Memory elements using this technology are composed of a thin film of silver doped chalcogenide or oxide glass sandwiched between a silver anode and an inert cathode. Under the influence of an electric field the electron current from the cathode reduces an equivalent number of Ag-ions as injected from the anode and a metal-rich electrodeposition is thereby formed in the electrolyte. The magnitude and duration of the ion current determines the amount of Ag deposited and hence the conductivity of the pathway. The electrodeposition is electrically neutral and stable; however, the formation process can be reversed by applying a bias with opposite polarity. The reverse ion current flows until the previously injected Ag has been oxidized (Ag → Ag$^+$ +e$^-$) and deposited back to the electrode which supplied the metal. Thus, the resistivity increases again until the high value of the solid electrolyte is reached. This resistive switching of the material caused by the formation and removal of the metallic Ag pathway can be used for information storage. Fig.1 shows a simplified illustration of the processes involved in WRITE and ERASE operations in this kind of memory elements. Due to its operation principle an element based on this technology is called a Programmable Metallization Cell or PMC.
Fig. 1: Schematic illustration of the electrodeposition process during WRITE (left side) and removal during ERASE (right side) in a solid state ionic cell.

2. LAYOUT AND PROCESSING OF TEST-CHIPS

For the electrical characterization of the PMC technology test-chips were designed and processed which utilize an active-in-via concept, see Fig. 2. The memory cell is a multi-layered structure consisting of a bottom electrode (the inert cathode), the active material (solid electrolyte), the top electrode (the oxidizable anode) and a top metallization for electrical contact. This stack is surrounded by a dielectric material for isolation and encapsulation. The layer structure of the investigated memory cell is detailed in Table 1.

![Cross-section of memory cell](image)

Fig. 2: Sketch of a cross-section of one memory cell.

The processing starts with standard CMOS tools and equipment to form the bottom electrode and the SiO₂ dielectric layer by chemical vapor deposition. Via structures are defined in the dielectric by DUV lithography and a subsequent etch process. A lift-off technique is used for the processing of the remaining stack. For that purpose a layer of resist is spun on and structured in alignment with the via holes on the preprocessed wafer. Subsequently, the Ge₃Se₇ solid electrolyte film is deposited by thermal evaporation of the base glass, followed by a first Ag film. A photodissolution process is carried out to drive around 33at% silver in the chalcogenide glass to complete the solid electrolyte formation, as is described in [4]. A second thin silver layer, which will serve as a source of Ag ions during electrical operation, is then deposited. Subsequently, a gold layer is evaporated in order to improve the electrical contact. A lift-off defines the top electrode stack, and the contact pads to the bottom electrode are opened by reactive ion etching through the SiO₂ layer.

<table>
<thead>
<tr>
<th>Material</th>
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<tr>
<td>Au metallization</td>
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<tr>
<td>Ag top electrode</td>
</tr>
<tr>
<td>Ag₀.₃₃Ge₀.₂₀Se₀.₄₇ active material</td>
</tr>
<tr>
<td>metal bottom electrode</td>
</tr>
<tr>
<td>SiO₂ dielectric layer</td>
</tr>
<tr>
<td>silicon substrate</td>
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Table 1: Materials used for the different layers of the test-chip devices.

By means of this processing scheme we have fabricated single devices with different feature sizes. The areas of the via holes (A) range from 5µm x 5µm rectangles down to 100nm diameter circles.

3. CURRENT-VOLTAGE MEASUREMENTS

The quasi-static IV characteristics of the test-chip devices are measured by probing the respective contact pads and connecting the tips to an Agilent 4156 Semiconductor Parameter Analyzer. Voltage double-sweeps are carried out starting at reverse bias conditions, ending at appropriate forward voltage values and sweeping back again. Current compliance levels were set in order to protect the device during switching. Fig. 3 shows typical IV curves obtained by applying this method. It should be noted, that all measurements have been done at room temperature.

The following important features can be derived from measured data. Instantaneous switching from a high-resistivity OFF-state to a low-resistivity ON-state occurs at approx. +240mV, defined as the threshold voltage Vth. Reversing the bias results in switching back to OFF-state at approx. -80mV. Typical OFF/ON ratios of the resistivity are as high as 10⁶. Multiple sweeps under the same conditions show only small variations in switching parameters. Normally, the virgin sweep (cycle1) reveals slightly greater deviations as can be seen in Fig. 3, which can be regarded as a necessary preconditioning for the
device. Thus, we have a memory device based on reproducible resistive switching at very low voltage with high OFF/ON ratio.

![IV-characteristic of a PMC device with A=1μm² measured at room temperature. The compliance level was set to 2μA. Three subsequent sweeps are plotted.](image)

We have examined the scaling of some characteristic values derived from the IV-curves depending on the cross-sectional area of via holes A. The resistance of the ON- and OFF-state was calculated from the current flow at +50mV and +100mV during down- and up-sweep, respectively. In Fig. 4 the values R(ON) and R(OFF) are plotted for various contact area sizes A.

![Resistance R(OFF) and R(ON) calculated from IV-sweeps as a function of area A.](image)

Additionally, for a given area A multiple sweeps and different cells were evaluated in order to give an idea of the distribution of R. As can be seen, R(ON) is not affected by A and values range from 30kΩ to ~200kΩ for the chosen compliance level of 2μA. In the OFF-state a homogeneous current flow through the entire area A of the active layer is expected. Hence, a variation of R(OFF) with 1/A is expected, and can be rudimentary detected for large area cells, see Fig. 4. At medium cell sizes the resolution of the measured data (max. ~10¹¹Ω) limits the R(OFF) values. The slight decrease in R(OFF) observable for the smallest via devices is due to poor step coverage caused by the deposition system. This leads to a thinner electrolyte film and therefore a smaller OFF-resistance.

4. MEMORY DEVICE CHARACTERISTICS

There are several reliability considerations associated with using a technology for data storage. Among others, retention and endurance are of great relevance.

The retention of the written ON-state and the erased OFF-state of PMC devices was measured. A typical result is illustrated in Fig. 5. The compliance level for the cell was set to 2μA, which gives a starting value R(ON) = 100kΩ.

![Typical retention of the ON-state: R(OFF) is well above 10¹⁰Ohm, as measured before and after retention test. The line is only a guide to the eye.](image)

As can be seen, there is an increase in resistance of the ON-state of the written cell. However, a linear extrapolation of the data still gives a sufficient resistance ratio of ~10² after 10 years. The cell was erased after testing and R(OFF) was well above 10¹⁰Ω, just as at the beginning of the test.

Endurance, i.e. the ability to withstand repeated program and erase cycles, is another important property for memory applications. In order to determine the PMC performance, a pulse-generator instead of the Parameter Analyzer was used to stimulate the samples. The voltage drop ΔV_R across an additional series resistor of 1kΩ was used as a measure of the current flow. Switching of the devices was achieved with a pulse-width as short as 200ns, a value which is limited by the RC-delay of the experimental setup and not by the material properties of the cell. For endurance measurements relatively long pulses (10μs WRITE, 50μs ERASE) were applied. During cycling, the switching of the cells was confirmed by monitoring ΔV_R on a digital oscilloscope. IV-curves were
measured after distinct time intervals in order to get detailed values of the switching parameters. A typical result is presented in Fig. 6, which shows a functional IV-curve after $10^5$ cycles and $V_{th}$, R(OFF), and R(ON) as a function of the number of cycles.

During the cycling test, the threshold voltage increases slightly from 250mV to 330mV, and R(ON) stays constant during cycling. R(OFF) shows a gradual reduction resulting in an OFF/ON-ratio of approx. $10^5$ after $10^5$ cycles.

5. SUMMARY AND CONCLUSION

In summary, the processing and characterization of memory elements based on resistive switching due to the formation and removal of Ag-rich pathways in solid electrolyte material was reported. Low voltage and current operation was demonstrated and high OFF/ON-ratios of many orders of magnitude have been achieved. The PMC devices scale well within the investigated feature sizes down to 100 nm. As is expected from the conducting mechanism in PMC devices, the OFF resistance depends inversely on the device area. In contrary, the ON resistance is determined by the conductive link formed during the electrochemical reaction during cell programming, and thus no area dependence is observed. As was reported in [5], this scaling of PMC devices can be extended well beyond 100 nm.

Linear extrapolation of retention data indicates that sufficient OFF/ON resistance margin is retained over 10 years, as is a requirement for nonvolatile operation.

Endurance measurements up to $10^5$ cycles reveal only a minor shift in the threshold voltage $V_{th}$ for device switching. However, limited cyclability/endurance was found under the chosen pulse parameters, which is comparable to standard Flash products. This is mainly caused by a decrease of the OFF resistance, while the ON resistance stays perfectly stable. However, it is expected, that a further optimization of the WRITE and ERASE conditions could lead to improved endurance behavior.

In conclusion, the investigated PMC devices reveal a low voltage switching and a retention behavior that makes these devices an attractive candidate for future nonvolatile memories.

6. REFERENCES


Fig. 6: Change of characteristic values during endurance test. Cycling of the cell was performed applying WRITE pulses (830mV / 10μs) and ERASE pulses (900mV / 50μs). The IV-curve shown in the lower part was measured after $10^5$ cycles.
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