Boise State University
Electrical and Computer Engineering Department
Course Syllabus for ECE 230
Digital Systems
Spring 2009

Instructor: Dr. S. M. Loo
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Office Hours: Monday and Wednesday, 10:00 AM -11:00 AM

Catalog Description:
Number systems, Boolean algebra, logic gates, Karnaugh mapping, combinatorial circuits, flip-flops, registers, counters, sequential state-machines, and small design projects.

Required text:

Text:

Simulation Software:
Xilinx ISE 10.1i

Time and Place: (Lecture) MWF 1:40 PM to 2:30 PM, ET 103
Lab: Tu 8:40 AM to 11:30 PM, MEC 311

Course Webpage: http://coen.boisestate.edu/smloo/ece230spring2009

Topics:
1. Introduction – Design Concepts
2. Introduction to Logic Circuits
3. Implementation Technology
4. Optimized Implementation of Logic Functions
5. Number Representation and Arithmetic Circuits
6. Combinational-Circuit Building Blocks
7. Flip-flops, Registers, and Counters
8. Synchronous Sequential Circuits

Prerequisites: COMPSCI 117 or COMPSCI 125

Grading (EE 230):
Test (2 @ 20% each) 40%
Final Exam 20%
Quiz 20%
Homework (includes Simulations) 20%

Grade determination: 100%-90% = A, 89%-80% = B, 79%-70% = C, 69%-60% = D, < 60% = F

Note and disclaimers:
There will be rough spots. Question and comments are expected and encouraged. Homework will be assigned during every lecture. Homework assigned of the week (Monday, Wednesday, and Friday) will be due the following Wednesday. It is due at beginning of class. NO LATE homework will be accepted. The latest list of homework problems will be posted on the class webpage.
**Code of Conduct:**
Discussing the assignments with other students is encouraged, as this could be one way to understand the materials. However, the work submitted must be your own. Copying from any source (from someone else, old files, or solution manual!) and turning it in is not permitted. Penalties for copying/cheating range from receiving a 0 on the assignment to receiving an F for the course.

*Student Code of Conduct, Article 3, Section 1, Academic Dishonesty*
Cheating or plagiarism in any form is unacceptable. The University functions to promote the cognitive and psychosocial development of all students. Therefore, all work submitted by a student must represent her/his own ideas, concepts, and current understanding. Academic dishonesty also includes submitting substantial portions of the same academic course work to more than one course for credit without prior permission of the instructor(s).

**Course Objectives:**
After taking this course, the students should be able:
- Calculate the functions described by logic diagrams
- Implement functions in logic gates and FPGA
- Reduce gates usage of a logic circuit implementation
- Develop proficiency in using Karnaugh maps, functional reduction, and data sheets
- Design circuits using state diagrams
- Develop logic circuits using combinational and clocked logic
- Design, simulate, and implement counter using state machine technique
- Design, simulate, and implement sequence detector

**Assessment Methods (Including Computer Usage and Design Content):**
- Exam: Two mid terms and one final exam will be given as scheduled
- Quiz: Quiz will be given every week
- Homework: Homework will be assigned every lecture to be collected the following Wednesday (to be graded and returned within one-week for timely review)

**Relationship of Course to Program Outcomes:**
The objectives of this course are:

**Contribution of Course to Meeting the Professional Component:**
Engineering Topics: 100%