Boise State University  
Electrical and Computer Engineering Department  
Course Syllabus for ECE 432/532 & Comp sci 441/541  
Computer Architecture  
Spring 2008

Instructor: Dr. S. M. Loo  
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Office Hours: Tuesday and Thursday, 2:00 PM - 4:00 PM

Catalog Description:  
This three-credit course demonstrates the computer architecture from the application programs down to the  
hardware levels. The tradeoffs between the instruction set, processor, memory, bus capacity, and peripherals will  
be examined. Details of memory hierarchy, clock cycle optimization and pipelining will be presented.  
Prerequisite: EE332 Microprocessors.

Required:  
David Patterson, John Hennessy, Computer Organization and Design, The Hardware/Software Interface, 3rd  

Time and Place: (Lecture) TTH 4:40 PM to 5:55 PM, MEC 114

Course Webpage: http://coen.boisestate.edu/smloo/caspring2008

Topics to be covered:  
• MIPS Instruction Set Architecture  
• Instruction format  
• SPIM  
• ALU Design  
• Understanding Performance  
• Data Path & Control Design  
• Multi-cycle Implementation  
• Pipelining  
• Data Hazards  
• Memory Hierarchies  
• Cache  
• Virtual memory  
• Networking, Storage, and Multiprocessors

Grading1:  
Midterm test 20%  
Final exam 20%  
Quiz 15%  
Paper2 15%  
Processor implementation 15%  
Project 15%

Grade determination: 100%-90% = A, 89%-80% = B, 79%-70% = C, 69%-60% = D, < 60% = F  
(+ and – will be used accordingly)

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1 Graduate students will be graded a little differently! You are also expected to work more problems during tests.  
2 Paper proposal will be due 3/20/2008, the paper is due the week before final.
Note and disclaimer:
There will be rough spots. Question and comments are expected and encouraged. Homework will be assigned and posted on the course webpage, but none will be collected (this will be discussed). You are strongly encouraged to work those problems. Read the textbook! As an encouragement, fill-in-the-blank questions will be in the quizzes, midterm, and final. No conversation will be allowed during lecture. If you disturb the lecture, you will be asked to leave the lecture room. If you have a question, ask the instructor. If you have something we need to discuss, let’s get the whole class involve.

Code of Conduct:
Discussing the assignments with other students is encouraged, as this could be one way to understand the materials. However, the work submitted must be your own. Copying from any source (from someone else, old files, or solution manual!) and turning it in is not permitted. Penalties for copying/cheating range from receiving a 0 on the assignment to receiving an F for the course.

Student Code of Conduct, Article 3, Section 1, Academic Dishonesty
Cheating or plagiarism in any form is unacceptable. The University functions to promote the cognitive and psychosocial development of all students. Therefore, all work submitted by a student must represent her/ his own ideas, concepts, and current understanding. Academic dishonesty also includes submitting substantial portions of the same academic course work to more than one course for credit without prior permission of the instructor(s).

Course Objectives:
After taking this course, the students should be able to:
• quantify and access the performance of a processor
• translate C to assembly and binary representations
• know how the instructions are used to control the datapath
• implement the processor features using hardware description language
• understand what is pipelining
• understand how pipelining can be used to improve performance
• describe and understand the processor memory hierarchy

Schedule:
• 2 weeks discussion of the MIPS ISA and basic ALU architectures
• 2 weeks pipelined datapath design issues
• 1 week talking about performance
• 2 weeks to learn Verilog
• 2 week memory hierarchies (Caches & Virtual memory) and memory design issues
• 2 weeks I/O design issues
• 2 weeks multiprocessor design issues